What is claimed is:

1. A semiconductor device including a differential level converter circuit that receives a first signal and outputs a second signal of a larger amplitude than an amplitude of the first signal, the differential level converter circuit comprises a first MISFET pair of N type for receiving the first signal; a second MISFET pair of N type for improving a withstand voltage of the first MISFET pair; a third MISFET pair of P type having cross-coupled gates for latching the second signal from output; and fourth MISFET of P type for cutting off a supply voltage,

wherein a film thickness of gate insulating films of the second MISFET pair is thicker than a film thickness of gate insulating films of the first MISFET pair;

wherein a film thickness of gate insulating films of the third MISFET pair is thicker than the film thickness of the gate insulating films of the first MISFET pair;

wherein a film thickness of gate insulating film of the fourth MISFET pair is thicker than the film thickness of the gate insulating films of the first MISFET pair;

wherein an absolute value of a threshold voltage of the second MISFET pair is smaller than an absolute value of a threshold voltage of the third MISFET pair; and

wherein an absolute value of a threshold voltage of the first MISFET pair is smaller than the absolute value of the threshold voltage of the third MISFET pair.

2. The semiconductor device according to Claim 1, wherein the gate insulating films of the second MISFET pair, the third MISFET pair and the fourth MISFET are formed in one process and the insulating films of the first MISFET pair are formed in another process.

3. The semiconductor device according to Claim 1, wherein the level converter circuit further comprises a first gate boosting circuit that boosts the first signal with the amplitude of the first signal to form a third signal with an amplitude bigger than the amplitude of the first signal so as to supply the third signal to one gate of the second MISFET pair; and

a second gate boosting circuit that boosts a phase-inverted signal of the first signal with the amplitude of the first signal to form a fourth signal with an amplitude bigger than the amplitude of the first signal so as to supply the fourth signal to the other gate of the second MISFET pair.

4. The semiconductor device according to Claim 1, wherein a source-drain path of one MISFET of each MISFET pair is connected in series and a source-drain path of the other MISFET of each MISFET pair is also connected in series, such that the second MISFET pair is arranged between the first MISFET pair and the third MISFET pair.

5. The semiconductor device according to Claim 1, wherein the gate insulating films of the first MISFET pair are made of a material with a dielectric constant higher than the dielectric constant of silicon dioxide.

6. The semiconductor device according to Claim 1, wherein the differential level converter circuit outputs a first differential output from one drain of the third MISFET pair and a second differential output from the other drain of the third MISFET pair, and

the semiconductor device further includes a level transition detector that detects and outputs a first-in-time edge transition of one of the first differential output and the second differential output.

7. The semiconductor device according to Claim 6, wherein the level transition detector includes an RS flip-flop, an inverter, an OR gate, a NAND gate, and fifth MISFET of N type for cutting off the supply voltage,

the first differential output is input to a first input node of the RS flip-flop and the inverter,

the second differential output is input to a second input node of the RS flip-flop and a first input node of the OR gate,

an output of the RS flip-flop is input to a second input node of the OR gate, and

an output of the OR gate and an output of the inverter are input to the NAND gate.

8. The semiconductor device according to claim 7, wherein the level transition detector includes seventh MISFET of P type for controlling output level of the level transition detector.

9. The semiconductor device according to Claim 8, wherein a control signal to control the fifth and sixth MISFETs is a complementary signal of a control signal to control the fourth MISFET.

10. The semiconductor device according to Claim 1,

wherein the first signal has an amplitude being defined between a low level of a first potential and a high level of a second potential,

wherein the second signal has an amplitude being defined between a low level of a first potential and a high level of a third potential,

wherein the differential level converter circuit outputs a first differential output from one drain of the third MISFET pair and a second differential output from the other drain of the third MISFET pair, and

wherein the semiconductor device further includes a second level converter circuit for receiving the first and second differential outputs and for outputting a third signal with an amplitude defined between a low level of a fourth potential being lower than the first potential and a high level of the third potential.